MEMORY DEVIC

Inventor: Shozo KAWABATA Appln. No.: Unknown Docket No.: 024016-00069

FIG. 1 CONCEPTUAL DIAGRAM ILLUSTRATING ERASE OPERATION

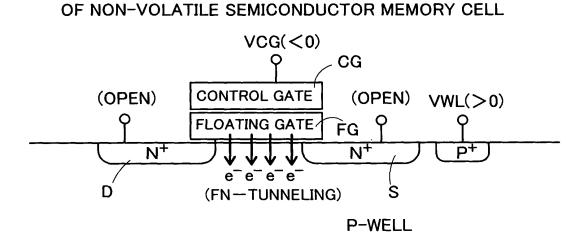
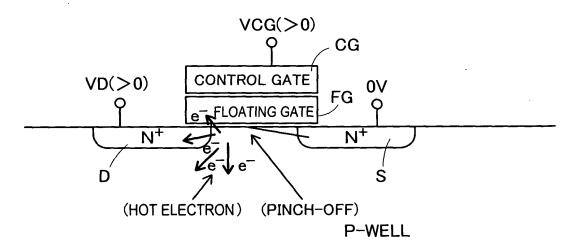


FIG. 2

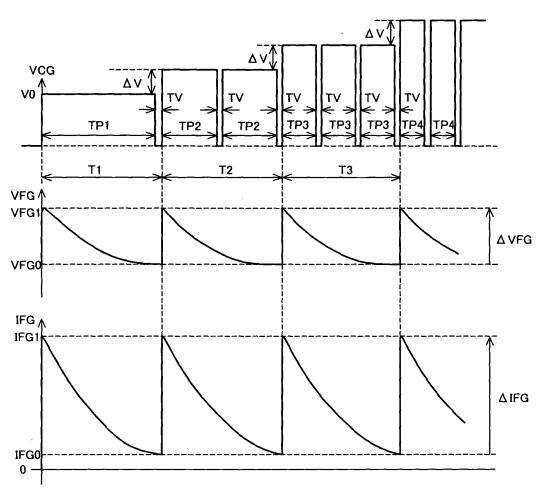
CONCEPTUAL DIAGRAM ILLUSTRATING WRITE OPERATION OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL



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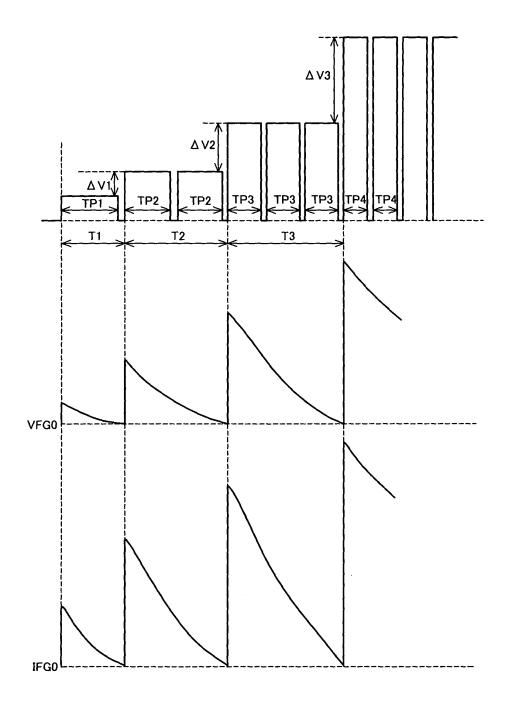
FIG. 3
WAVEFORM DIAGRAM DIRECTED TO FIRST EMBODIMENT



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FIG. 4
WAVEFORM DIAGRAM DIRECTED TO VARIANT OF FIRST EMBODIMENT



Title: CONTROL METHOD OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL AND NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

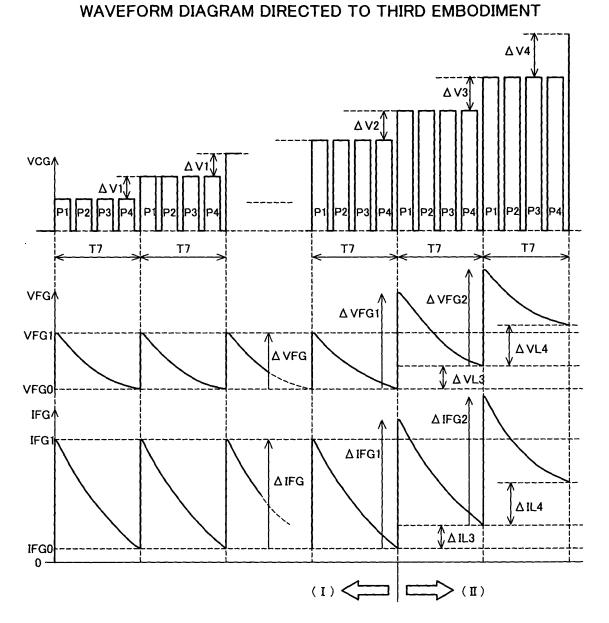
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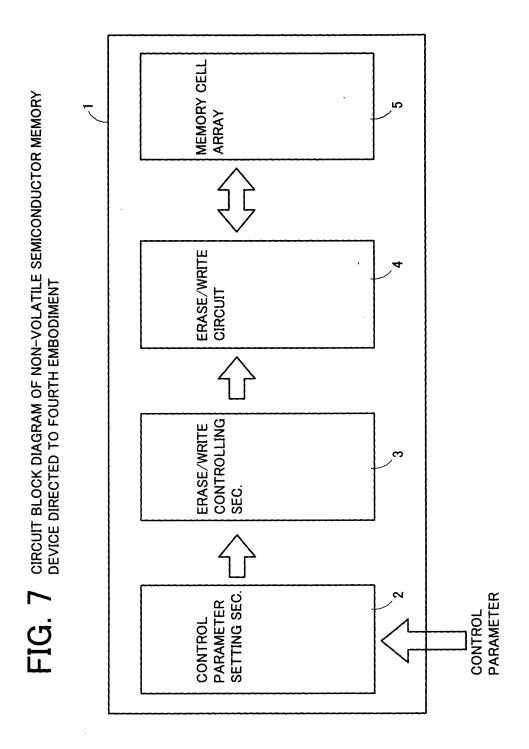
ΔVFG ΔIFG Ы A VL2 FIG. 5 WAVEFORM DIAGRAM DIRECTED TO SECOND EMBODIMENT <u>2</u> , A IL 2 91 P2 Ξ ₹ A VL1 ∬ ∆ 1L1 P3 P2 딥 P5 <u>P</u> P3 P2 P2 Р P5 \\\ P3 ᆵ VFG0<mark>-</mark> IFG ≜ VFG A 17.00 VFG1 IFG1

Title: CONTROL METHOD OF NON-VOLATILE SEMICONDUCTOR MEMORY CELL AND NON-VOLATILE SEMICONDUCTOR

MEMORY DEVICE Inventor: Shozo KAWABATA Appln. No.: Unknown Docket No.: 024016-00069

FIG. 6





Title: CONTROL METHOD OF NON-YOUR SEMICONDUCTOR MEMORY CELL AND NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

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